ABSTRACT OF THE DISCLOSURE

A method and apparatus for disabling the scan output of flip-flops contained within an integrated circuit. Registers within the integrated circuit form a serial shift register chain when in the test mode of operation. The registers contain therein flip-flops, each of the flip-flops having at least one data input, a scan test input, a data output, and a scan output. The flip-flop is capable of storing either the signal appearing on the at least one data input or the signal appearing on the scan test input, based on the mode of operation of the flip-flop. The flip-flop includes a circuit coupled between the data output and the scan output for selectively disabling the scan output from following the value of the data output. Consequently, the scan output is enabled to output the logic value stored in the flip-flop when the flip-flop is in the test mode of operation and is disabled from outputting the logic value stored in the flip-flop when the flip-flop is in the normal mode of operation. When the scan output is disabled from following the data output, the scan output is driven to a predetermined logic value.